



**Clean Version of Pending Claims**

**SILICON CARBIDE GATE TRANSISTOR**

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*Claims 1-5, 8-15, 22, 24-29, 31-35, 37-48, 50-53 and 55-57, as of April 23, 2001  
(response to office action filed).*

1.(Three Times Amended) A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising a source region, a drain region, and a channel region between the source and drain regions in a semiconductor surface layer formed on an underlying insulating portion, and an electrically interconnected gate formed of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ , wherein  $x$  is less than 0.5, the gate being connected to receive an input signal;

addressing circuitry to address memory cells in the array; and

control circuitry to control read, write, and erase operations of the memory device.

2.(Amended) The system of claim 1 wherein the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide.

3.(Amended) The system of claim 1 wherein:

the semiconductor surface layer comprises p-type silicon;

the gate is separated from the channel region by gate oxide or tunnel oxide;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

4.(Amended) The system of claim 1 wherein:

the semiconductor surface layer comprises n-type silicon;

the gate is separated from the channel region by gate oxide or tunnel oxide;  
the source region comprises p-type silicon; and  
the drain region comprises p-type silicon.

5.(Amended) The system of claim 1 wherein the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  is p+ doped with boron or n+ doped with phosphorus.

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6.(Amended) The system of claim 1 wherein:  
the addressing circuitry further comprises:

a row decoder; and  
a column decoder;

the memory device further comprises a voltage control switch; and

the system further comprises control lines, address lines, and data lines coupled between the processor and the memory device.

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7.(Amended) The system of claim 1 wherein the gate is separated from the channel region by an insulating layer that is approximately between 50 angstroms and 100 angstroms thick.

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8.(Amended) The system of claim 7 wherein the insulating layer is approximately 100 angstroms thick.

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9. An integrated circuit device comprising:  
a substrate;  
a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the p-channel transistor comprising a silicon carbide

compound  $\text{Si}_{1-x}\text{C}_x$ , wherein  $x$  is less than 0.5, and being connected to receive a first input signal;  
and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the n-channel transistor comprising a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ , wherein  $x$  is less than 0.5, and being connected to receive a second input signal.

<sup>10</sup>  
~~12~~. The integrated circuit device of claim <sup>9</sup>~~11~~, wherein the p-channel and n-channel silicon carbide gates comprise polycrystalline silicon carbide.

<sup>11</sup>  
~~13~~. The integrated circuit device of claim <sup>9</sup>~~11~~, wherein the p-channel and n-channel silicon carbide gates comprise microcrystalline silicon carbide.

<sup>12</sup>  
~~14~~. The integrated circuit device of claim <sup>9</sup>~~11~~, wherein the insulating layers, which separate the silicon carbide gates in each of the n-channel and p-channel transistors from their respective channel regions, are comprised of silicon dioxide.

<sup>13</sup>  
~~15~~. A semiconductor memory device comprising:  
a memory array including a plurality of transistors, at least one of the transistors in a semiconductor surface layer formed on an underlying insulating portion and including an electrically interconnected gate formed of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ , wherein  $x$  is less than 0.5, the gate being connected to receive an input signal;  
addressing circuitry to address the memory array; and  
control circuitry to control read, write, and erase operations of the memory device.

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<sup>14</sup>  
~~22~~. The integrated circuit device of claim <sup>9</sup>~~1~~ wherein the substrate comprises a semiconductor surface layer formed on an underlying insulating portion.

<sup>15</sup>  
24. The semiconductor memory device of claim <sup>13</sup>~~15~~ wherein a plurality of the transistors in the memory array comprise:

a source region, a drain region, and a channel region between the source and drain regions in a semiconductor surface layer formed on an underlying insulating portion; and

an electrically interconnected gate formed of a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ , wherein  $x$  is less than 0.5, the gate being connected to receive an input signal.

<sup>16</sup>  
25. The semiconductor memory device of claim <sup>13</sup>~~15~~ wherein pairs of the transistors in the memory array comprise:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the p-channel transistor comprising a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ , wherein  $x$  is less than 0.5, and being connected to receive a first input signal; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the n-channel transistor comprising a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ , wherein  $x$  is less than 0.5, and being connected to receive a second input signal.

<sup>17</sup>  
~~26~~. The semiconductor memory device of claim <sup>16</sup>~~25~~ wherein the substrate comprises a semiconductor surface layer formed on an underlying insulating portion.

<sup>18</sup>  
~~27~~. The semiconductor memory device of claim <sup>13</sup>~~15~~ wherein the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises polycrystalline silicon carbide.

<sup>19</sup>  
~~28~~. The semiconductor memory device of claim <sup>13</sup>~~15~~ wherein the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises microcrystalline silicon carbide.

<sup>20</sup>  
~~29~~. The semiconductor memory device of claim <sup>13</sup>~~15~~ wherein the gate is separated from the semiconductor surface layer by an insulating layer of silicon dioxide.

<sup>21</sup>  
~~31~~. A semiconductor memory device comprising:  
a memory array including a plurality of transistors wherein pairs of the transistors comprise:

a substrate;

a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the p-channel transistor comprising a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ , wherein  $x$  is less than 0.5, and being connected to receive a first input signal; and

an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the n-channel transistor comprising a

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silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$ , wherein  $x$  is less than 0.5, and being connected to receive a second input signal;

addressing circuitry to address the memory array; and

control circuitry to control read, write, and erase operations of the memory device.

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22. The semiconductor memory device of claim 21 wherein the substrate comprises a semiconductor surface layer formed on an underlying insulating portion.

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23. The semiconductor memory device of claim 21 wherein each silicon carbide gate comprises polycrystalline silicon carbide.

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24. The semiconductor memory device of claim 21 wherein each silicon carbide gate comprises microcrystalline silicon carbide.

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25. The semiconductor memory device of claim 21 wherein each insulating layer comprises silicon dioxide.

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26. (Twice Amended) A memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising:

a substrate having a source region, a drain region, and a channel region between the source region and the drain region formed in the substrate;

an insulating layer on the substrate over the channel region; and

a gate comprising a p+ doped silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer, wherein  $x$  is less than 0.5, the gate being electrically interconnected to receive an input signal.

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28. (Twice Amended) The memory device of claim 27 wherein:

the substrate comprises a silicon surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the silicon surface layer;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  is p+ doped with boron; and

further comprising:

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device.

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29. (Amended) The memory device of claim 27 wherein:

the substrate comprises p-type silicon;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

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30. (Amended) The memory device of claim 27 wherein:

the substrate comprises n-type silicon;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

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~~31~~. (Twice Amended) A memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising:

a substrate having a source region, a drain region, and a channel region between the source region and the drain region formed in the substrate;

an insulating layer on the substrate over the channel region; and

a gate comprising an n+ doped silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer, wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

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~~32~~. (Twice Amended) The memory device of claim ~~31~~ wherein:

the substrate comprises a silicon surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the silicon surface layer;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  is n+ doped with phosphorus; and

further comprising:

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device.

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~~43~~. (Amended)

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The memory device of claim ~~41~~ wherein:

the substrate comprises p-type silicon;  
the source region comprises n-type silicon; and  
the drain region comprises n-type silicon.

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~~44~~. (Amended)

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The memory device of claim ~~41~~ wherein:

the substrate comprises n-type silicon;  
the source region comprises p-type silicon; and  
the drain region comprises p-type silicon.

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~~45~~. (Twice Amended) A memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising:

a source region, a drain region, and a channel region between the source region and the drain region formed in a semiconductor substrate;

an insulating layer on the semiconductor substrate over the channel region; and

a gate comprising a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer

wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

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~~46~~. (Amended)

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The memory device of claim ~~45~~ wherein:

the semiconductor substrate comprises a p-type silicon surface layer formed on an underlying insulating portion;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

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The memory device of claim 45 wherein:

the semiconductor substrate comprises an n-type silicon surface layer formed on an underlying insulating portion;

the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the insulating layer comprises gate oxide or tunnel oxide;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

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48.(Twice Amended) The memory device of claim 45 wherein the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  is p+ doped with boron or n+ doped with phosphorus.

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50.(Twice Amended) A system comprising:

a processor; and

a memory device coupled to the processor, the memory device comprising:

an array of memory cells comprising a plurality of transistors, at least one of the transistors comprising:

a source region, a drain region, and a channel region between the source region and the drain region formed in a semiconductor substrate;

an insulating layer on the semiconductor substrate over the channel region;

and

a gate comprising a silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  on the insulating layer wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

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~~39~~. (Twice Amended) The system of claim ~~38~~ wherein:

the semiconductor substrate comprises a p-type silicon surface layer formed on an underlying insulating portion;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the source region comprises n-type silicon; and

the drain region comprises n-type silicon.

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~~40~~. (Amended) The system of claim ~~38~~ wherein:

the semiconductor substrate comprises an n-type silicon surface layer formed on an underlying insulating portion;

the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;

the insulating layer comprises gate oxide or tunnel oxide;

the source region comprises p-type silicon; and

the drain region comprises p-type silicon.

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~~41~~. (Twice Amended) The system of claim ~~38~~ wherein the silicon carbide compound  $\text{Si}_{1-x}\text{C}_x$  is p+ doped with boron or n+ doped with phosphorus.

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42 ~~34~~. The memory device of claim ~~34~~, further comprising:

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device.

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56. The system of claim 50 wherein:

the memory device further comprises:

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device; and

the system further comprises control lines, address lines, and data lines coupled between the processor and the memory device.

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A system comprising:

a processor; and

a memory device coupled to the processor through control lines, address lines, and data lines, the memory device comprising:

an array of memory cells comprising a plurality of transistors, each of the transistors comprising:

a source region, a drain region, and a channel region between the source region and the drain region formed in a semiconductor substrate;

an insulating layer on the semiconductor substrate over the channel region; and

means for controlling current in the channel region based on an input signal;

a row decoder coupled to the array;

a column decoder coupled to the array;

a voltage control switch; and

control circuitry coupled to the array to control read, write, and erase operations of the memory device.

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